

FIG.1

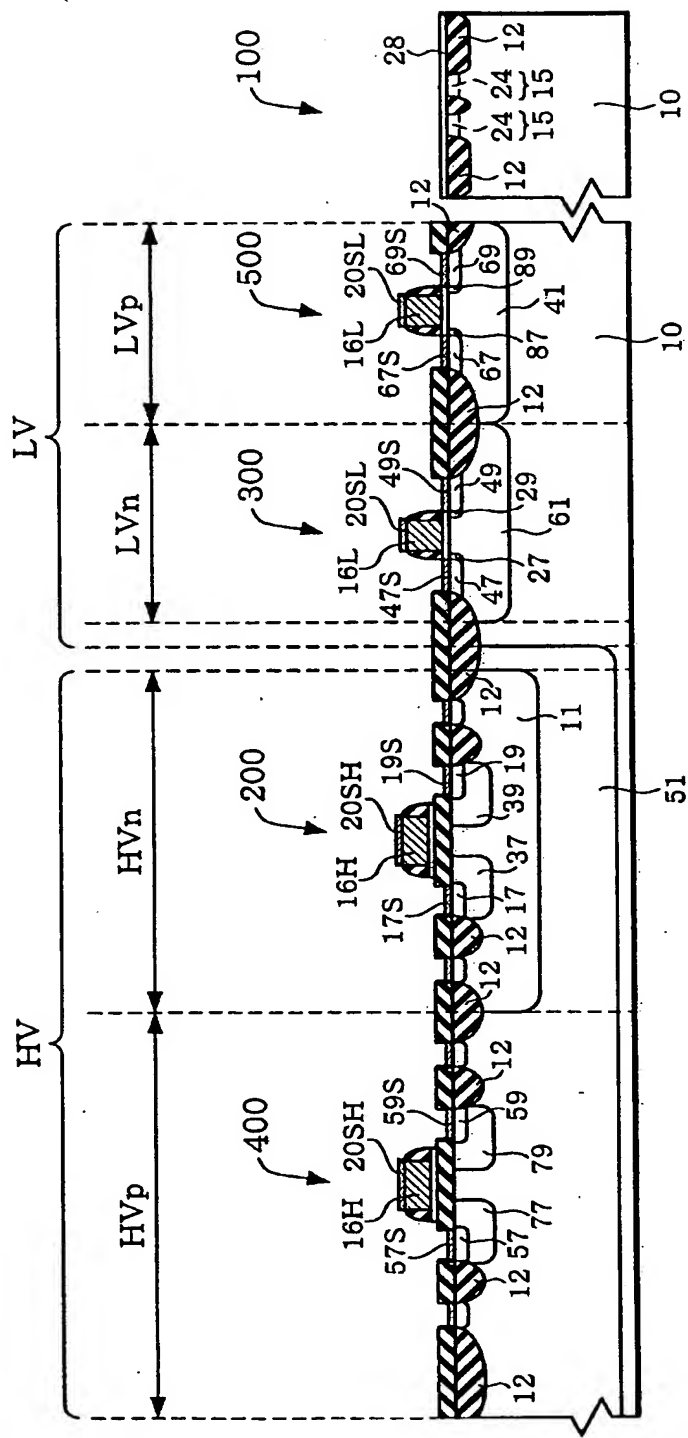


Figure 1 illustrates three cross-sectional views of a semiconductor device, labeled 200, 300, and 100, showing the progression of a manufacturing process.

View 200: Shows a substrate 10 with a layer 11. A patterned layer 13 is formed on the substrate. A layer 17 is formed on the patterned layer 13. A central region 18H is covered by a layer 16H, with side regions 18H and 28H. A layer 20SH is formed on top of the central region 18H.

View 300: Shows the same structure as view 200, but with additional layers 16L, 18L, and 20SL, and a layer 47S. The central region 18H is now covered by a layer 16L, with side regions 18L and 28L. A layer 20SL is formed on top of the central region 18L.

View 100: Shows the same structure as view 300, but with a layer 70 formed on top of the central region 18L. The central region 18L is now covered by a layer 70, with side regions 18L and 28L. A layer 24 is formed on top of the central region 18L.

FIG.3

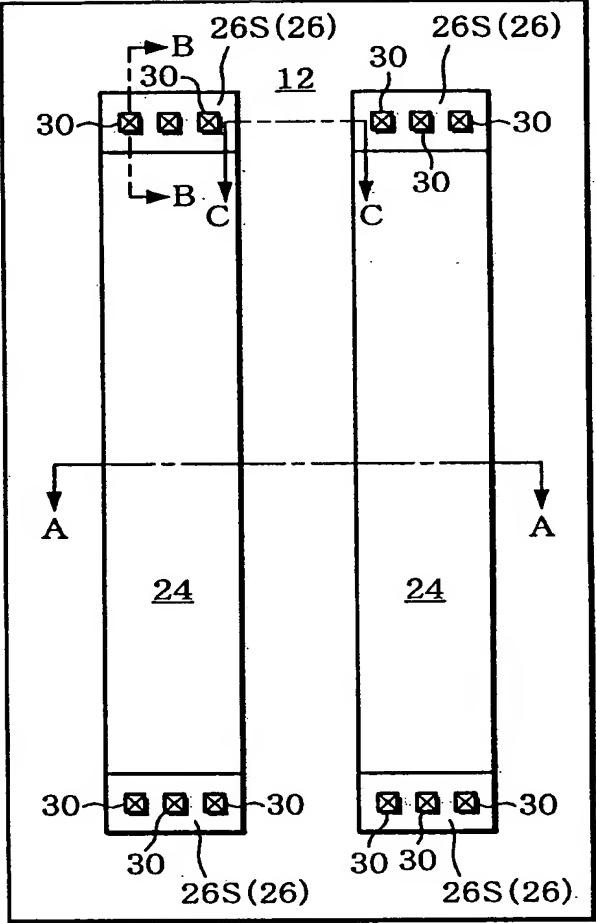


FIG.4

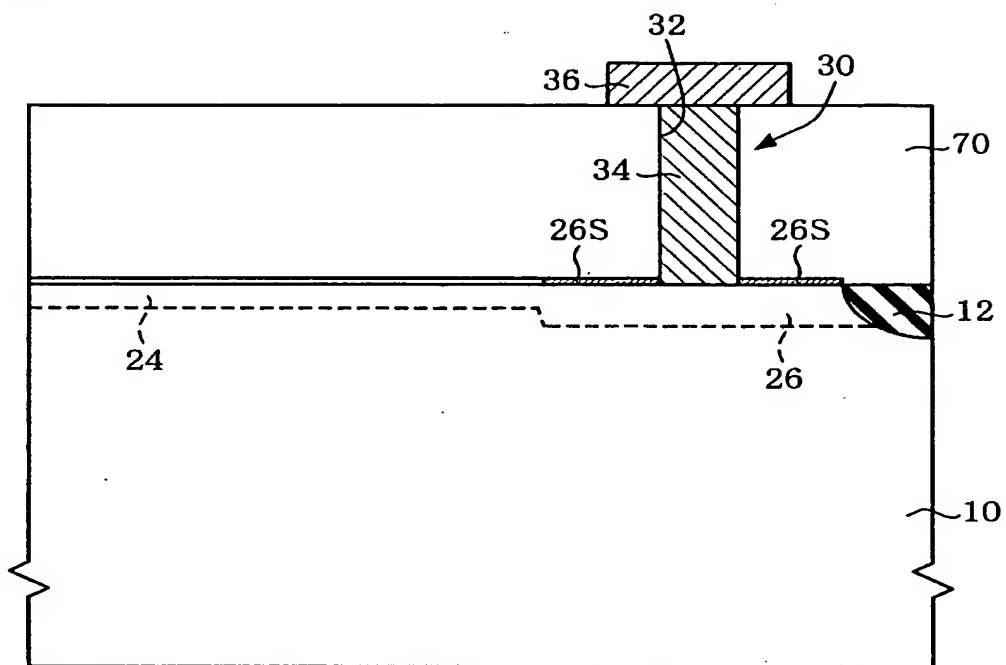


FIG.5

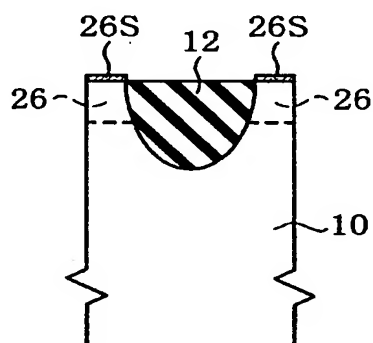


FIG.6

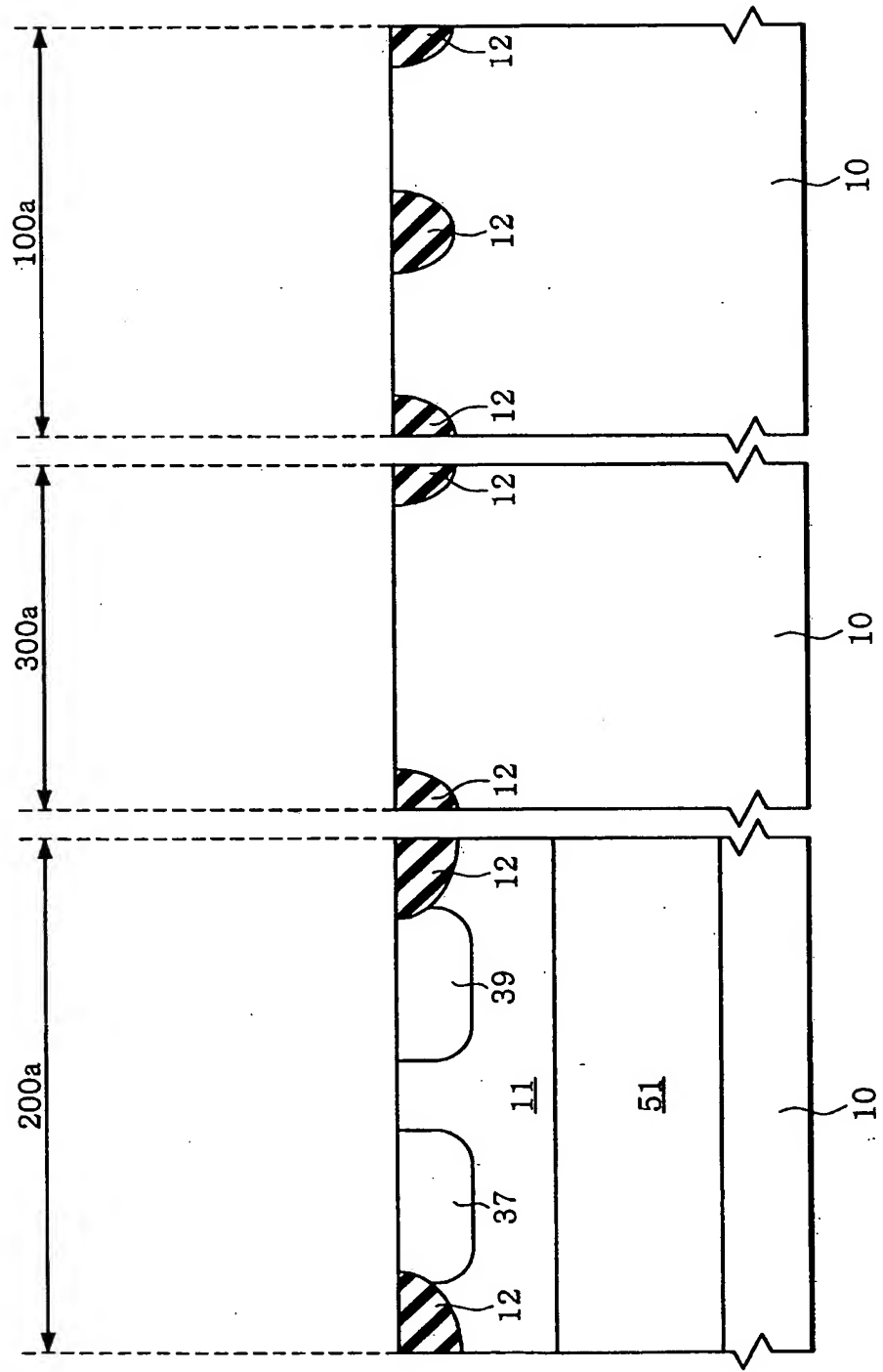


FIG.7

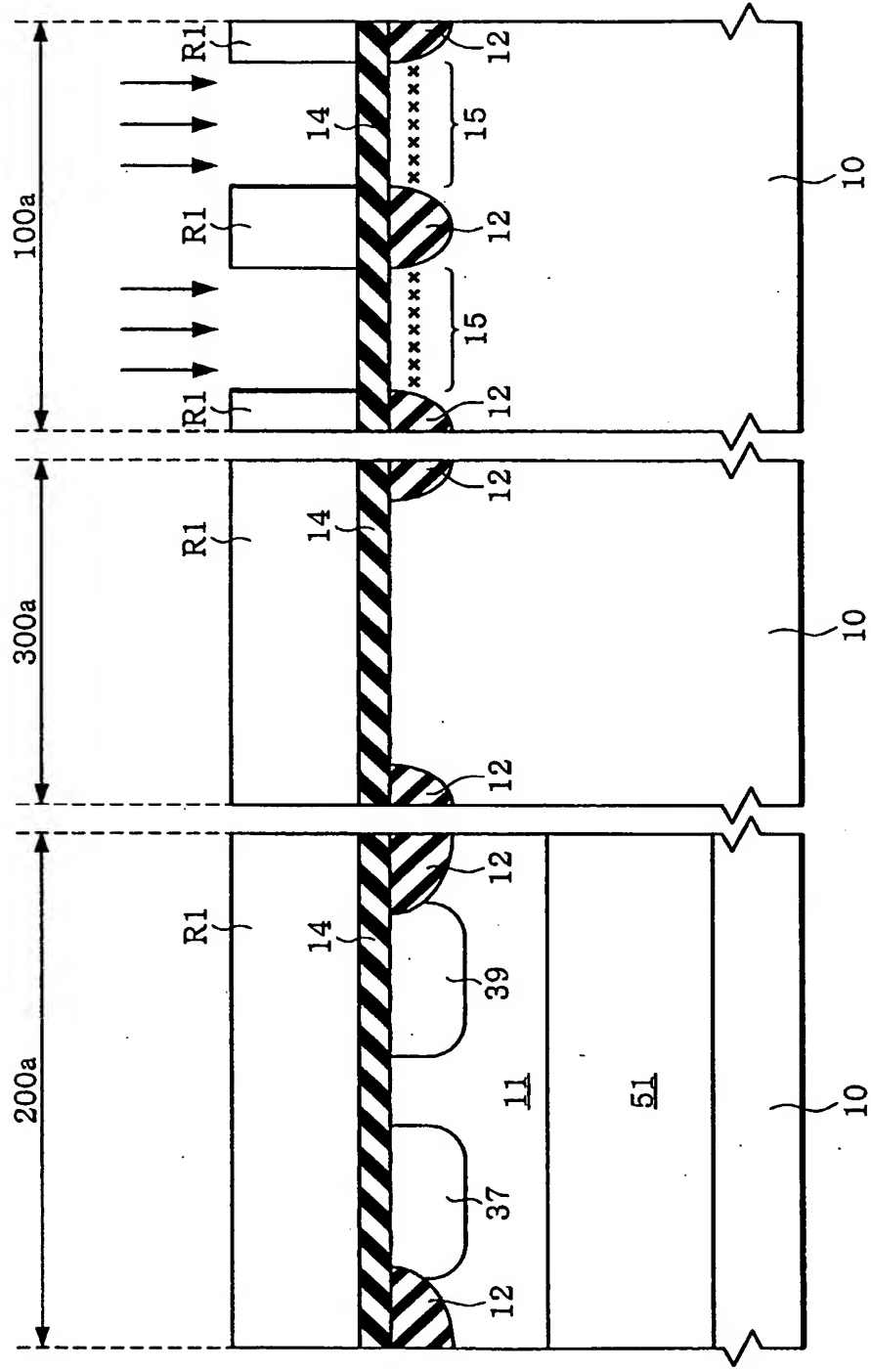


FIG.8

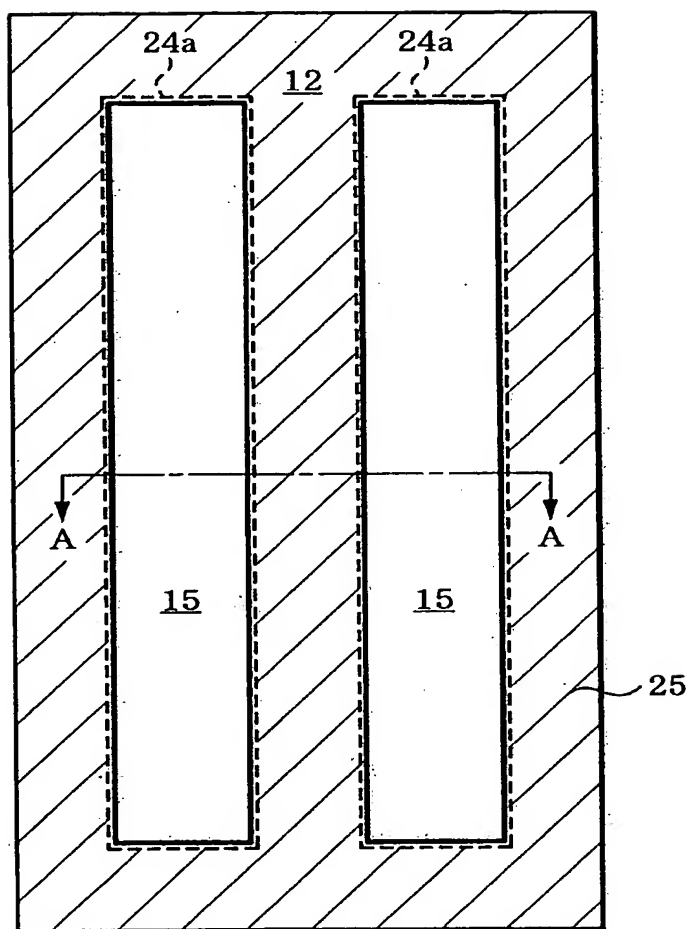


FIG.9

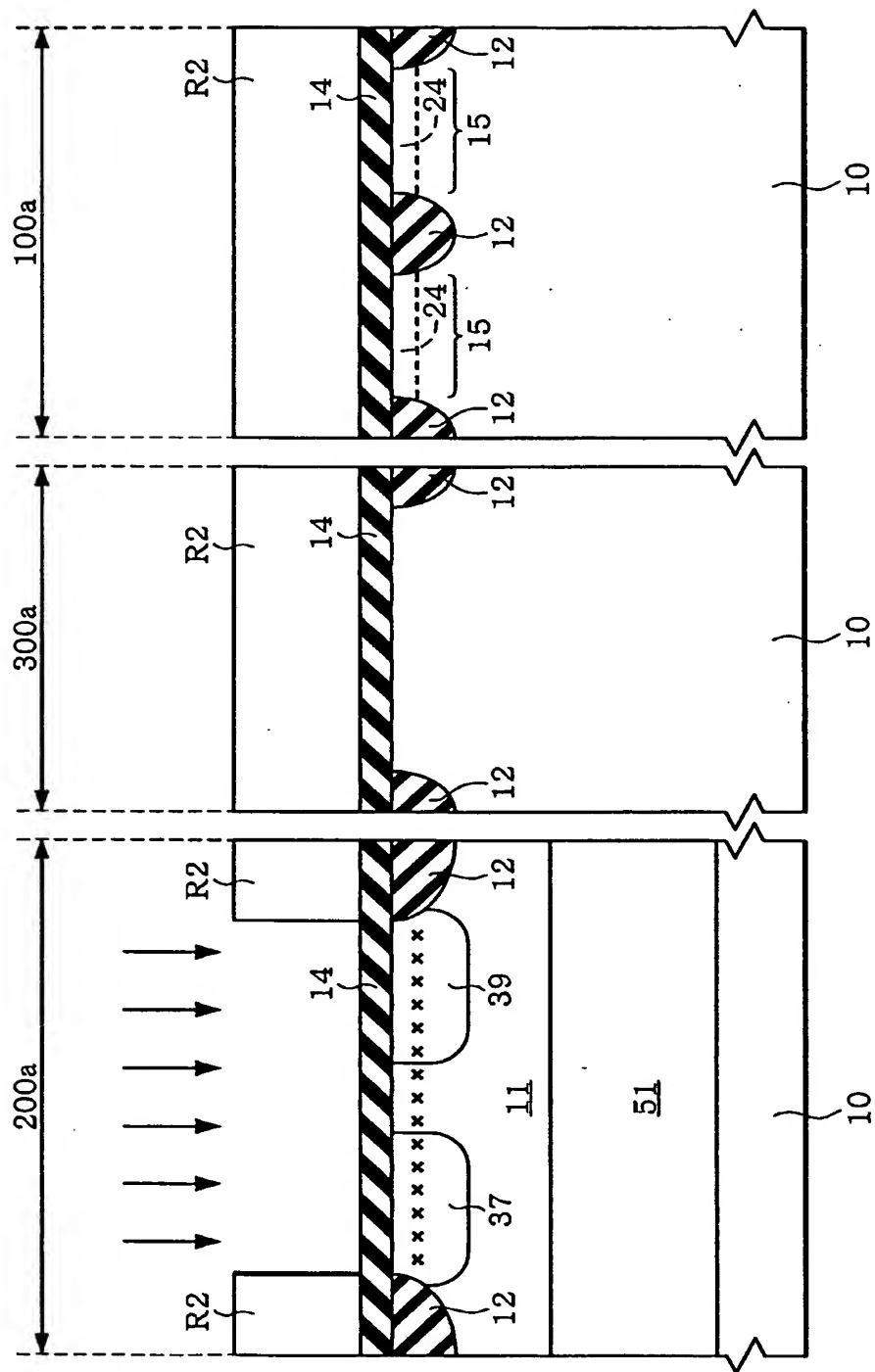


FIG.10

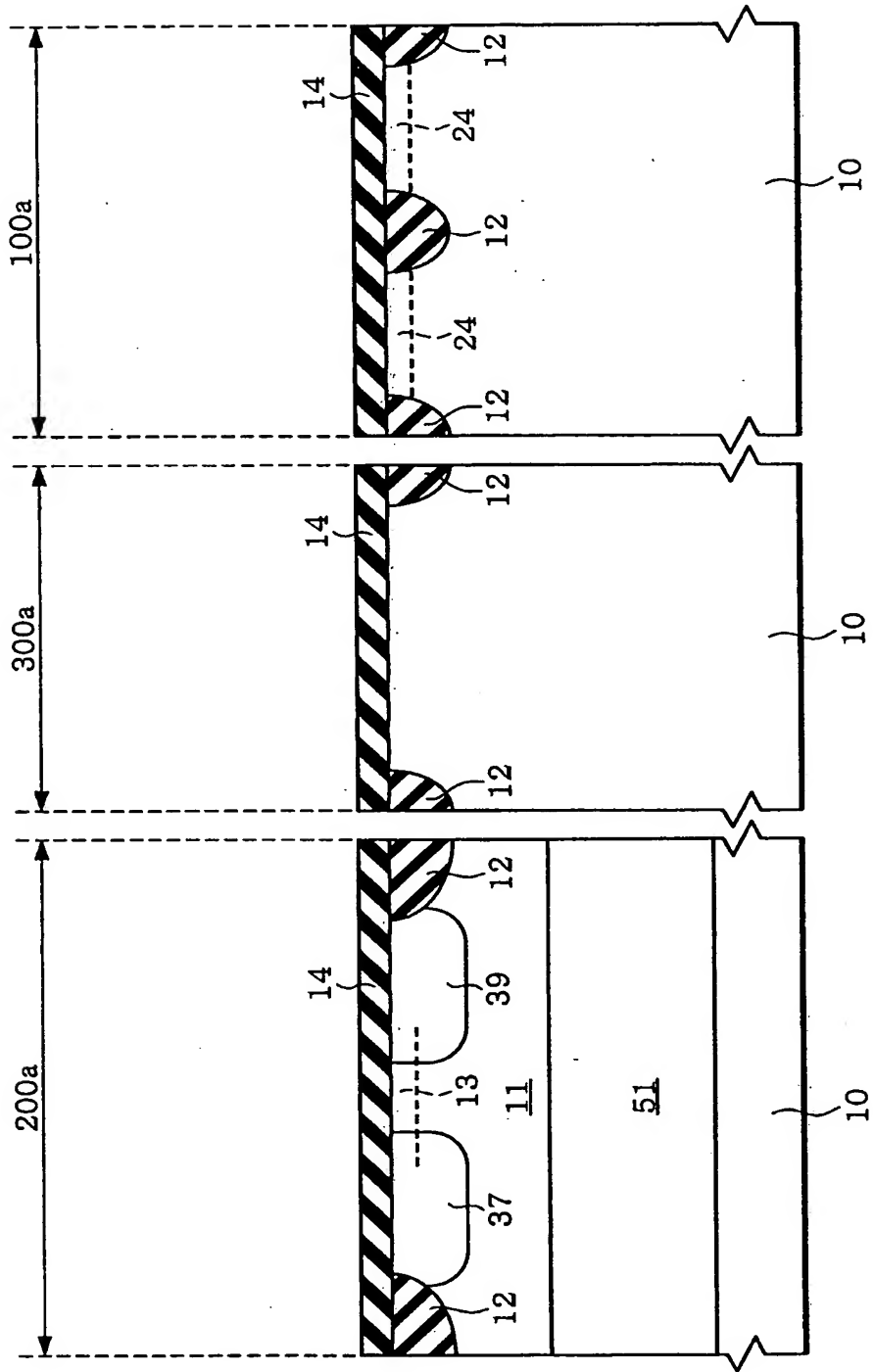


FIG.11

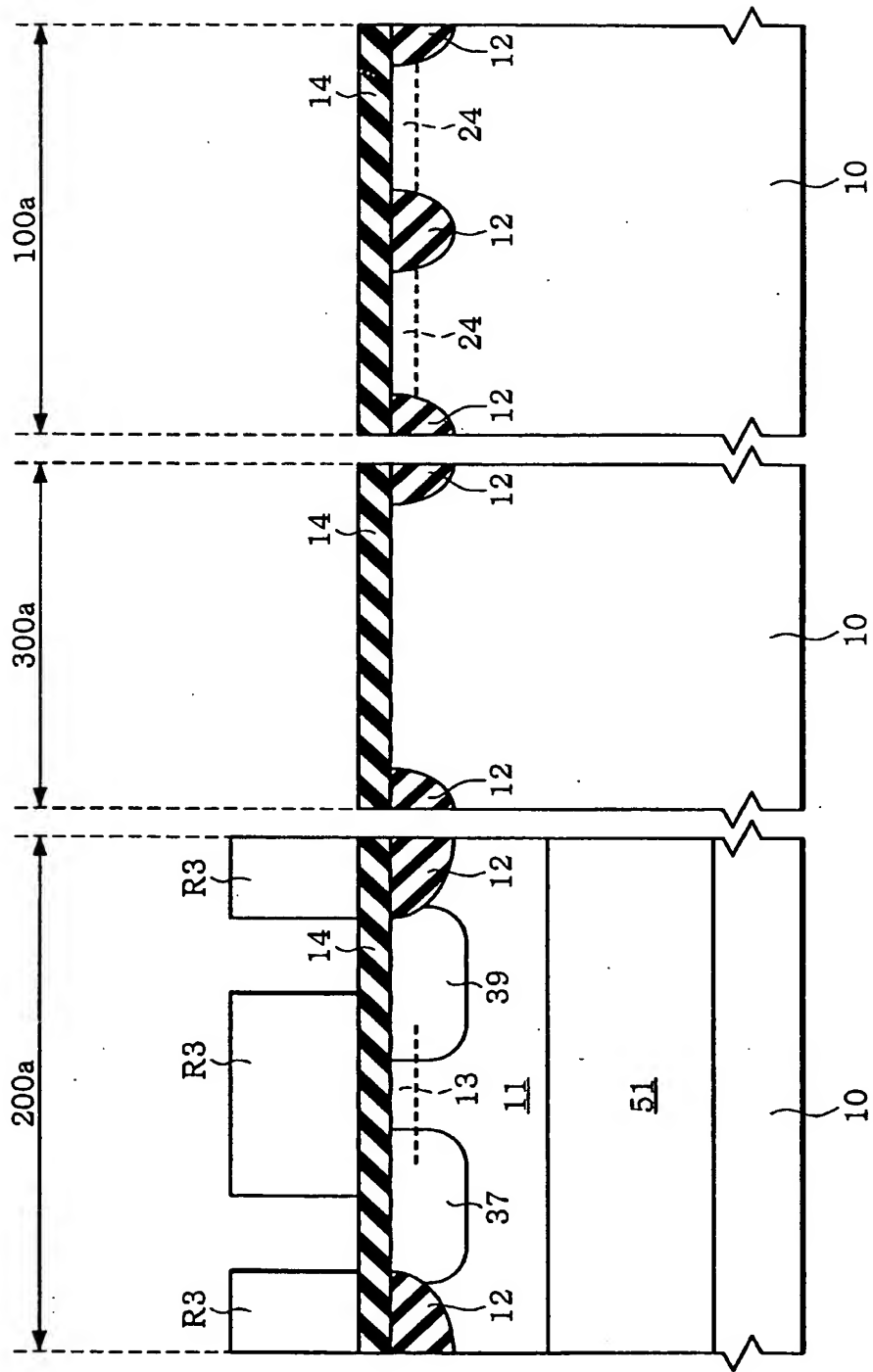


FIG.12

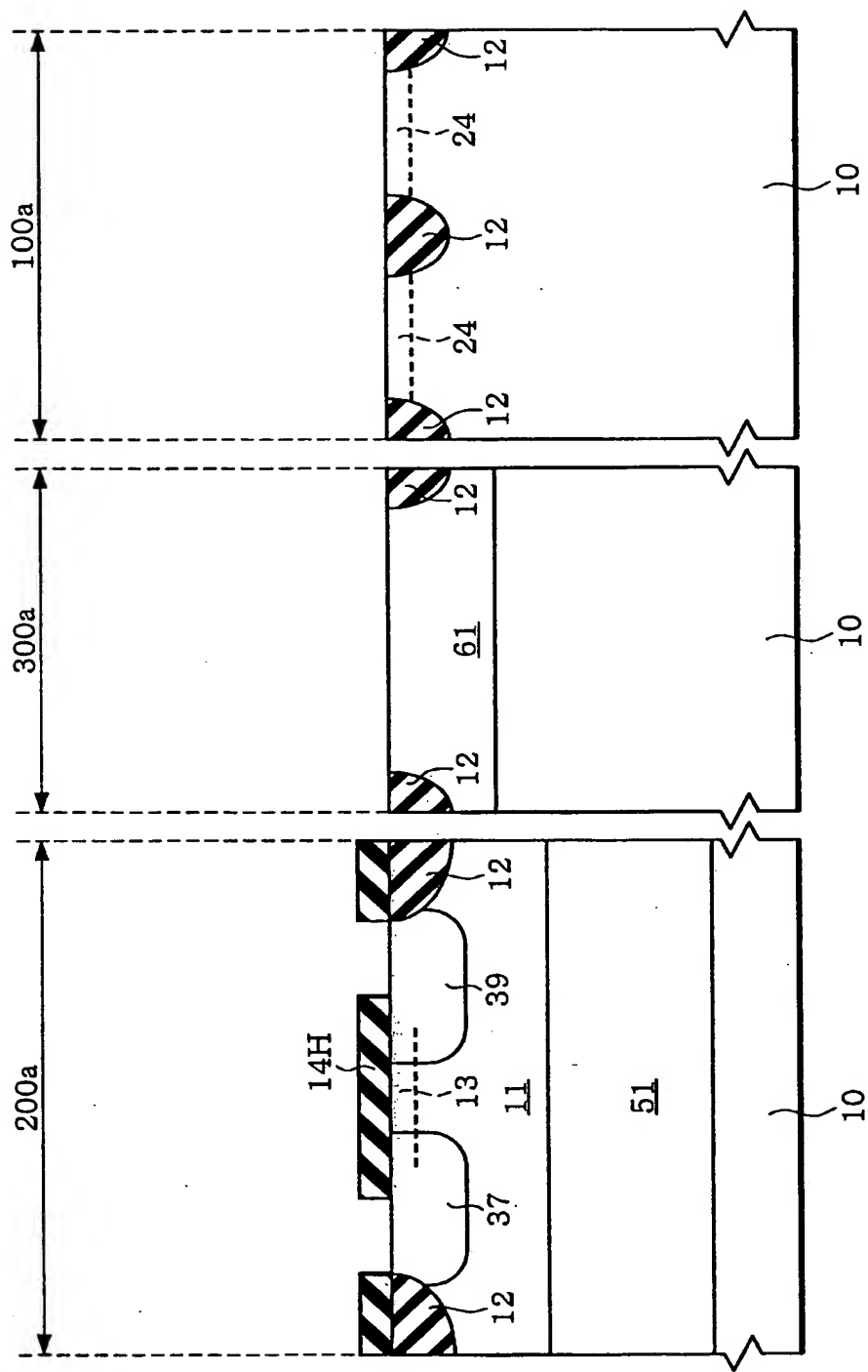


FIG.13

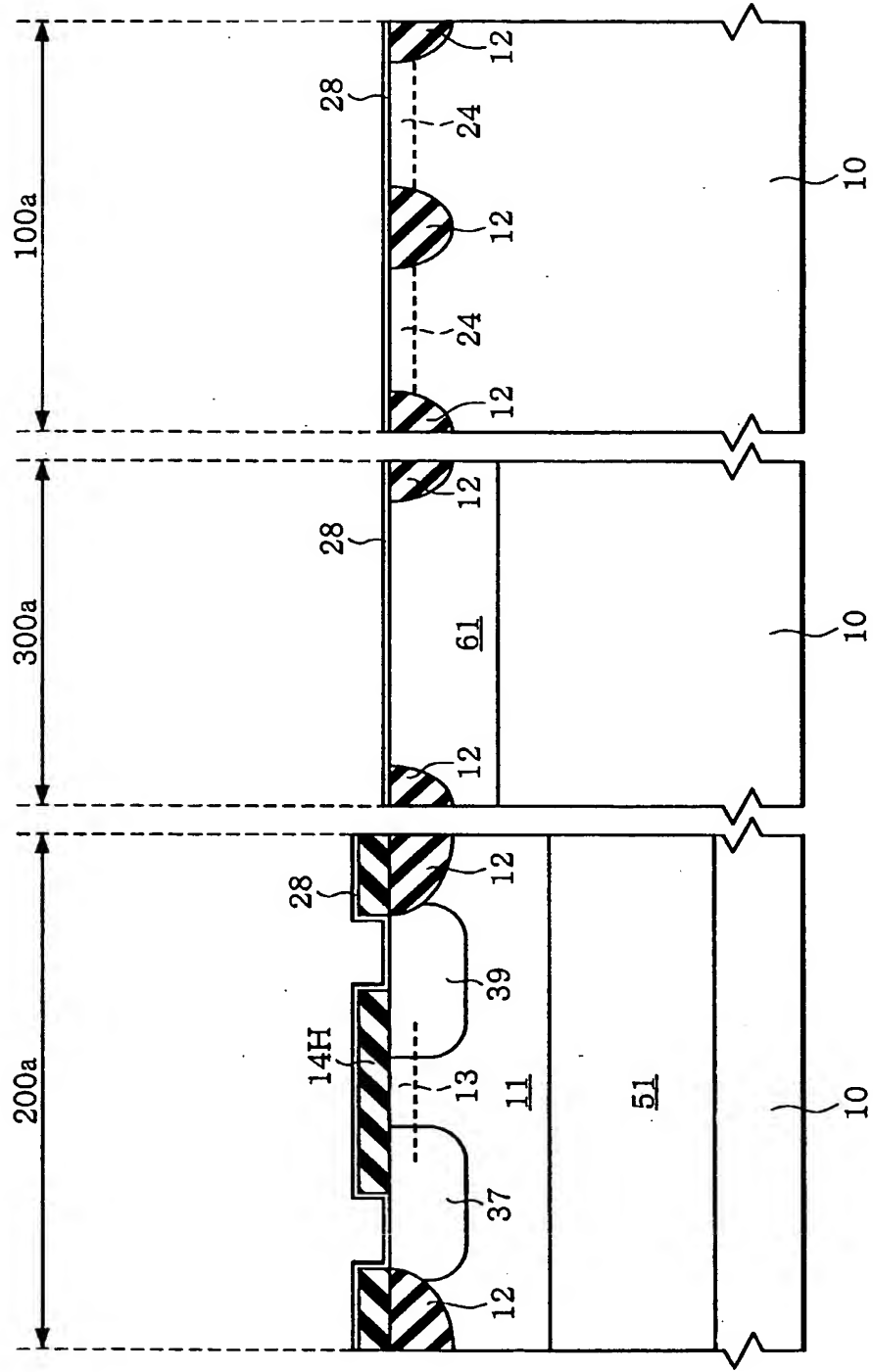


FIG.14

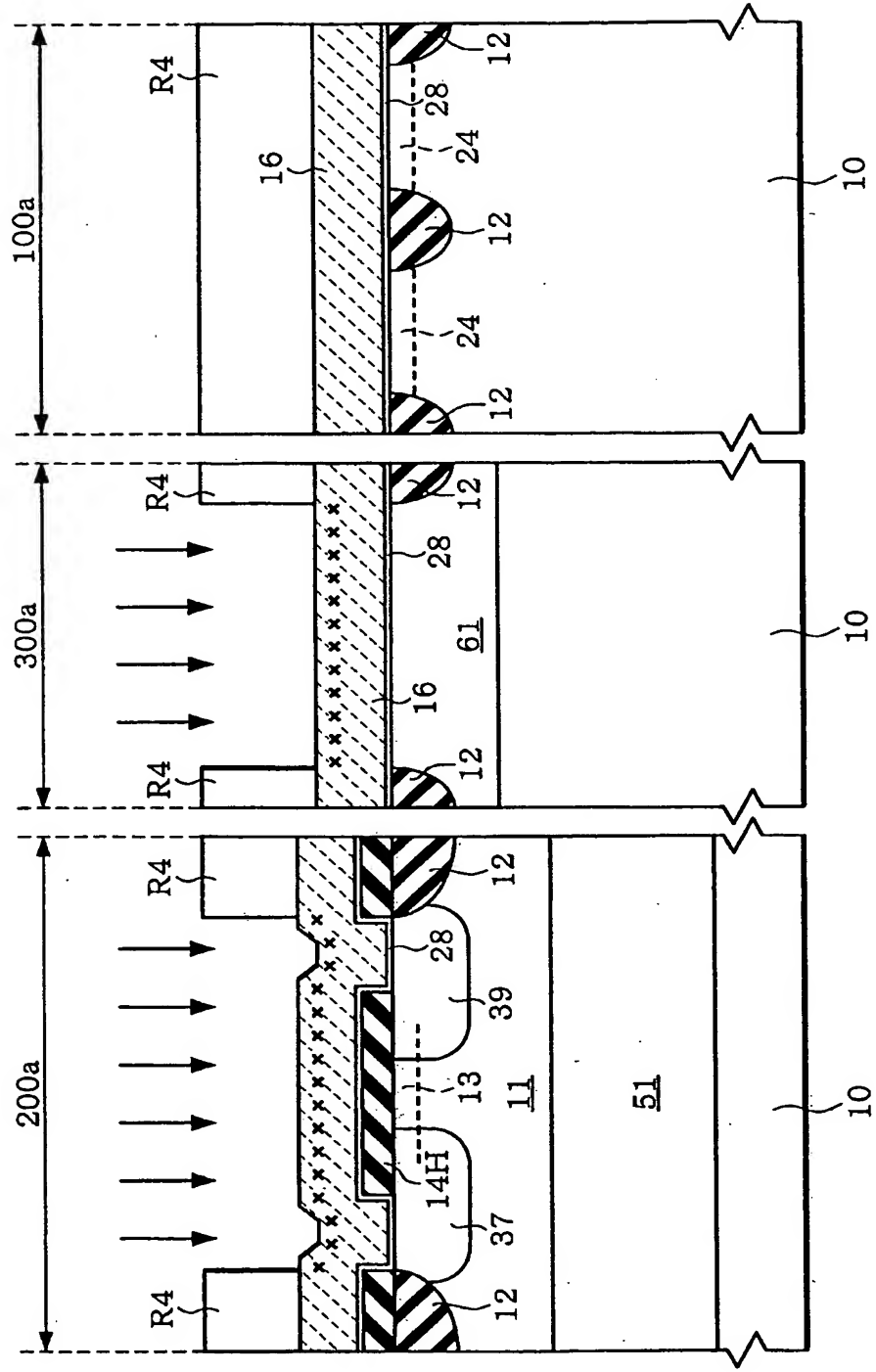


FIG.15

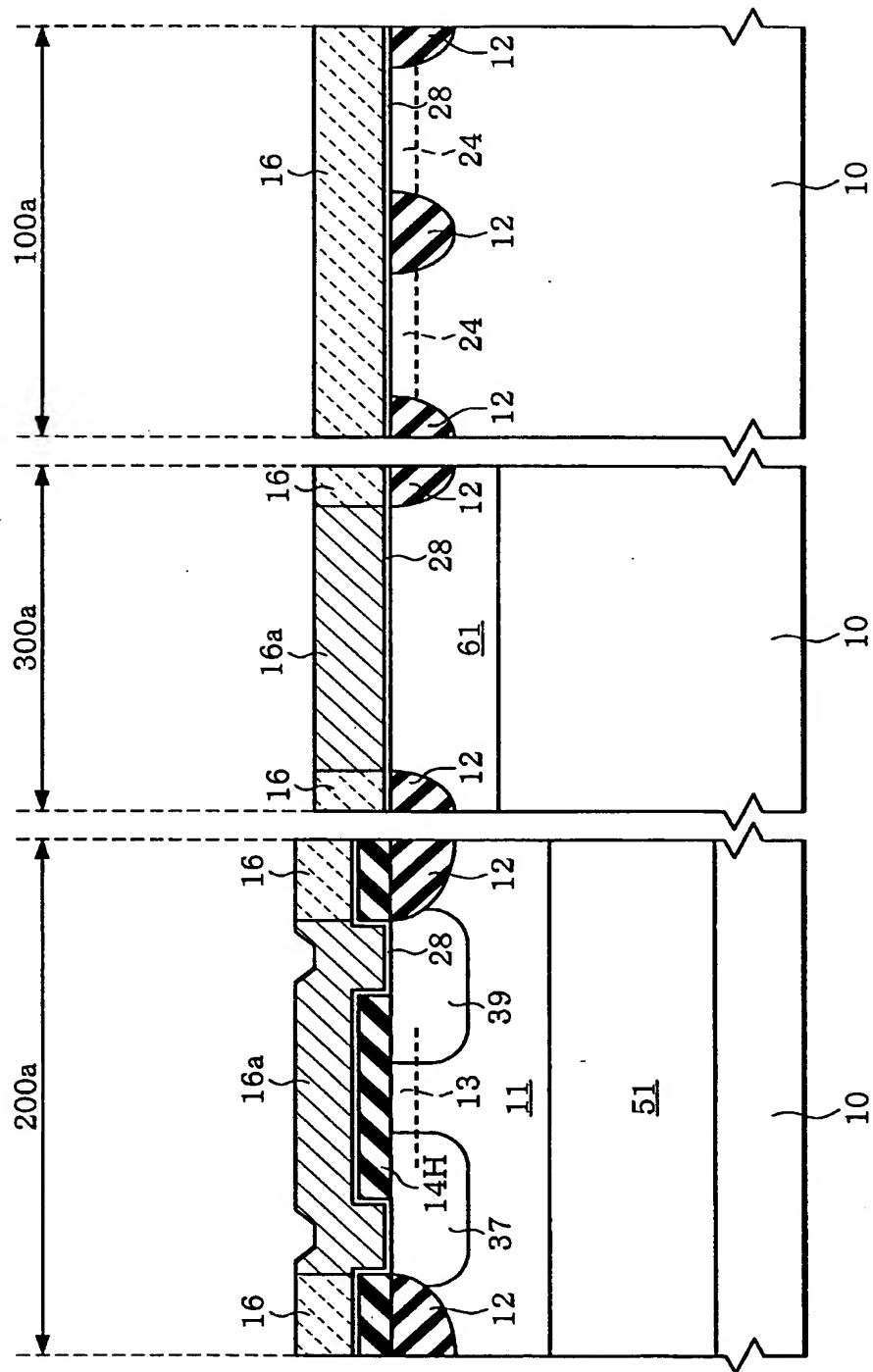


FIG.16

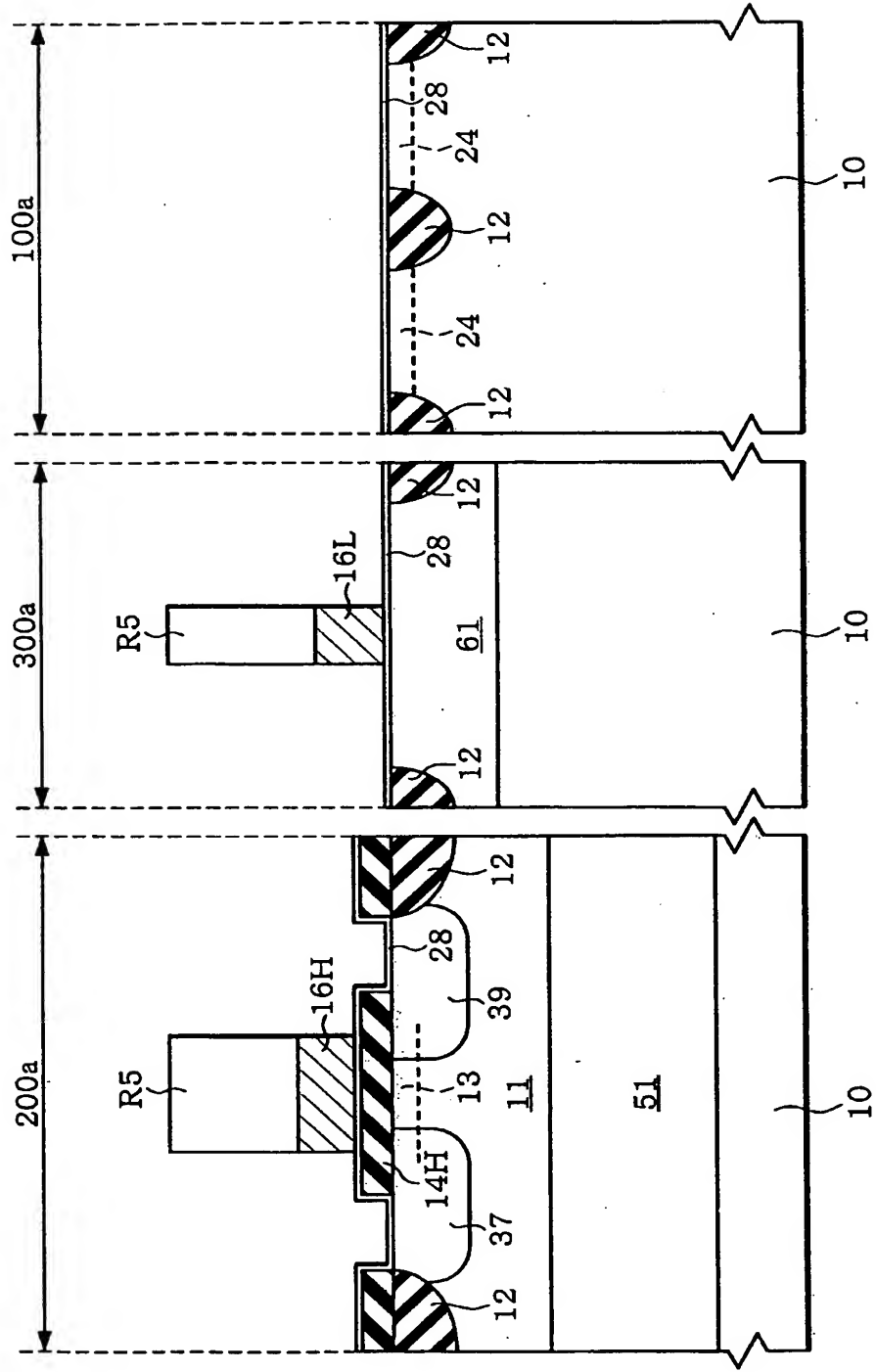


FIG.17

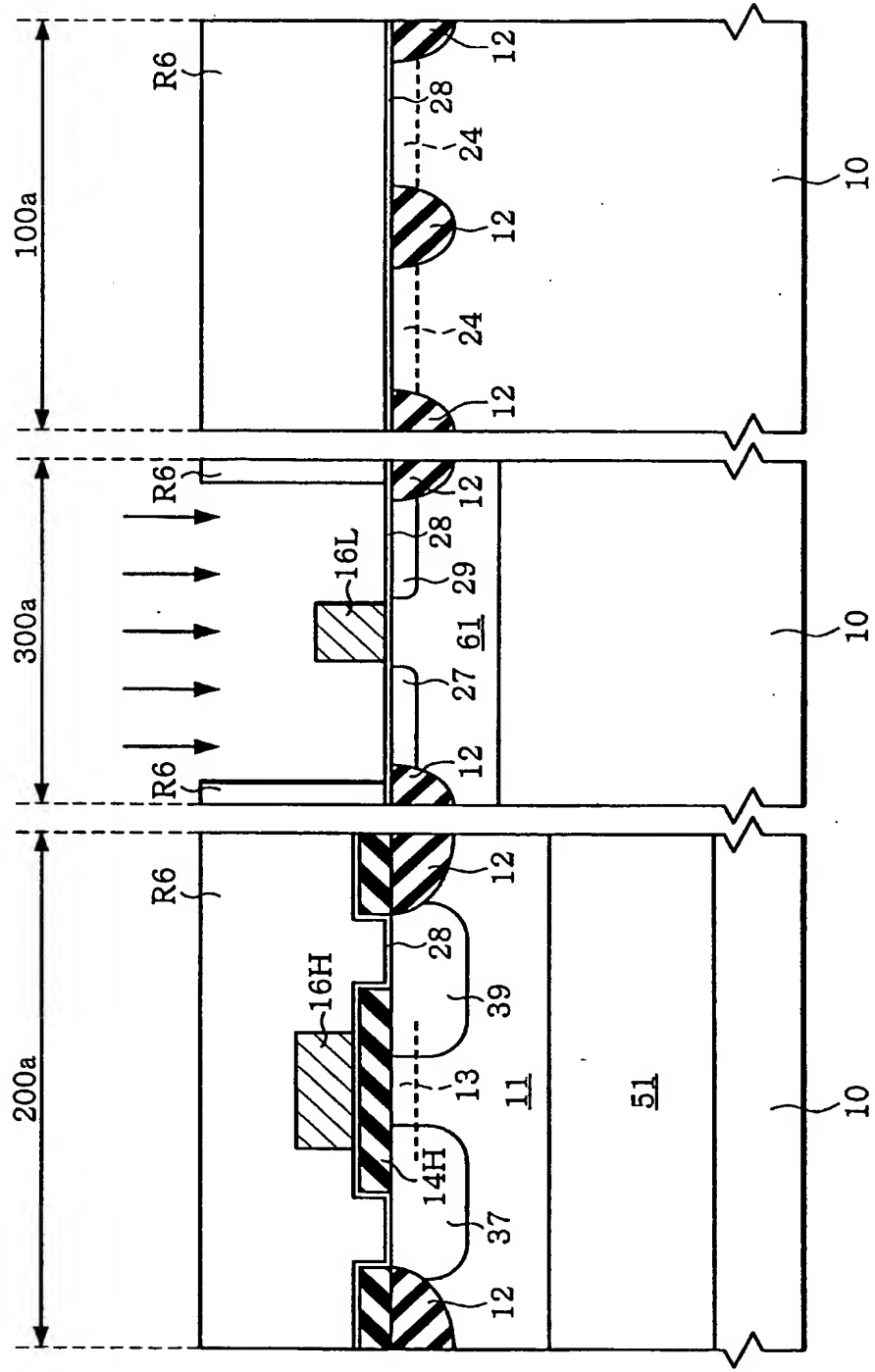


FIG.18

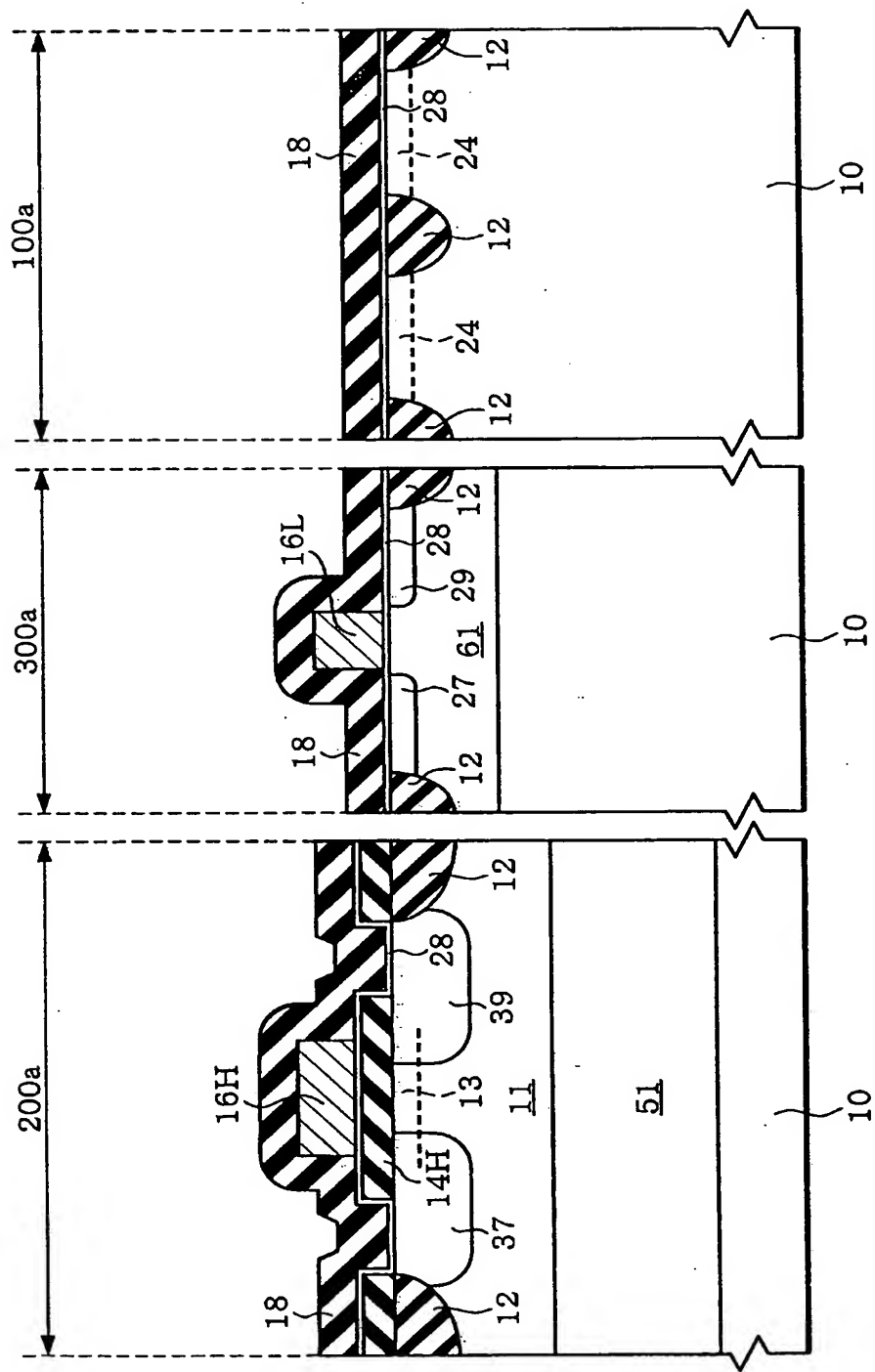


FIG.19

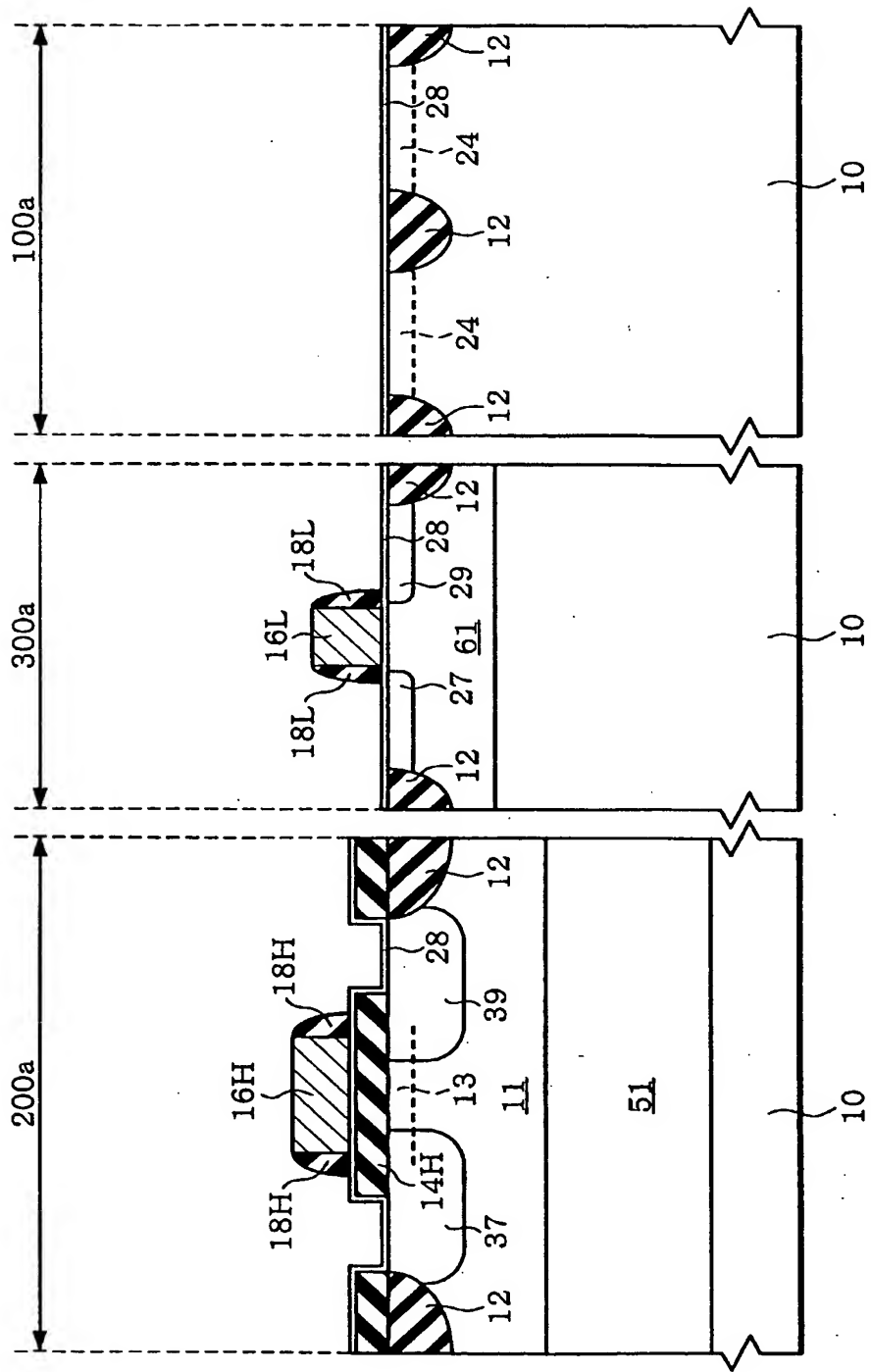


FIG.21

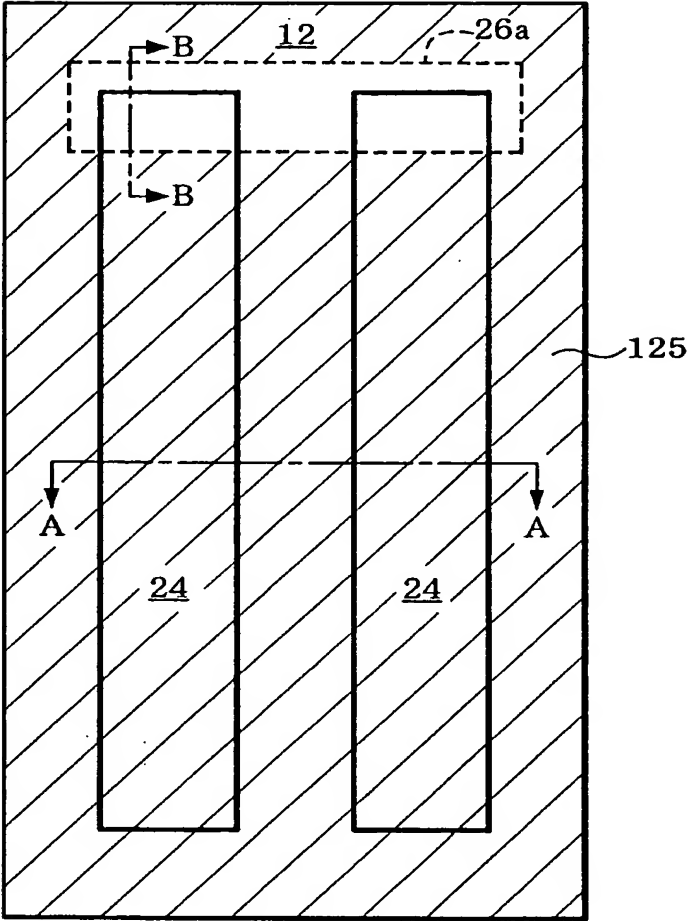


FIG.22

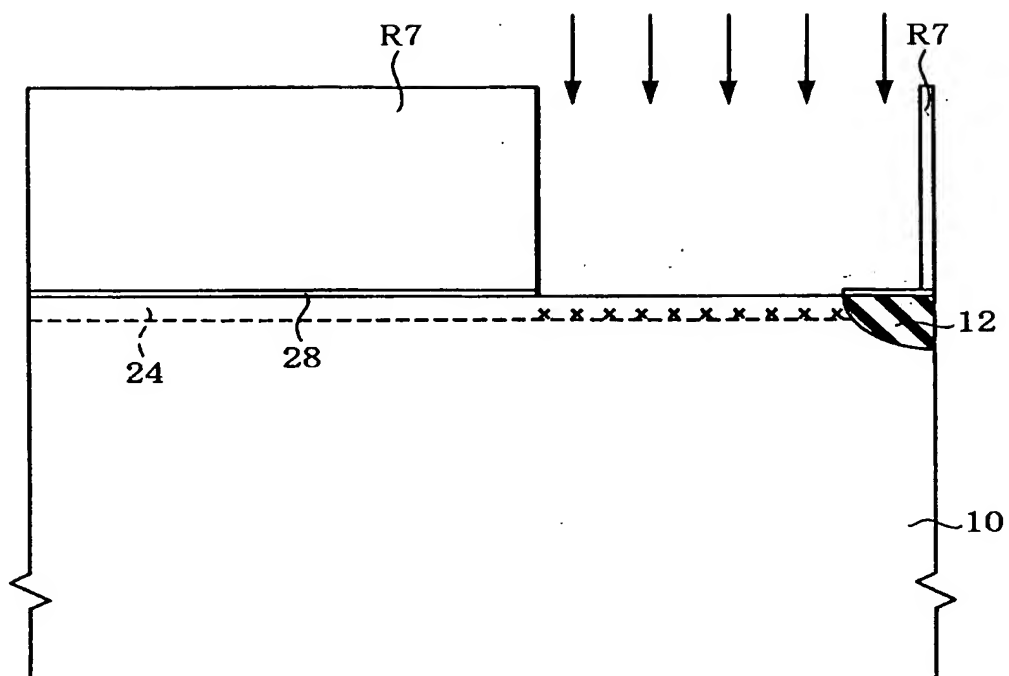


FIG.23

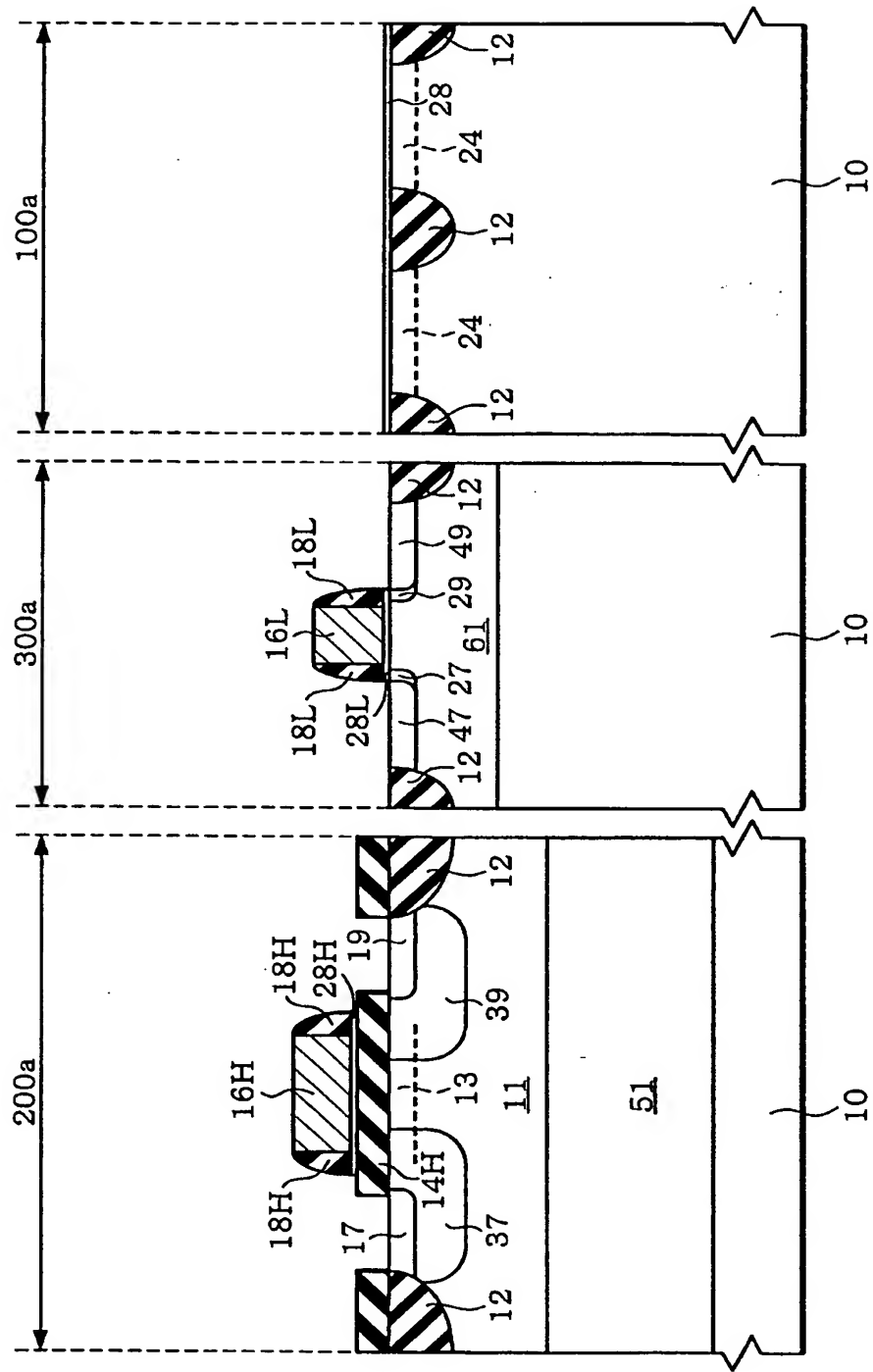


FIG.24

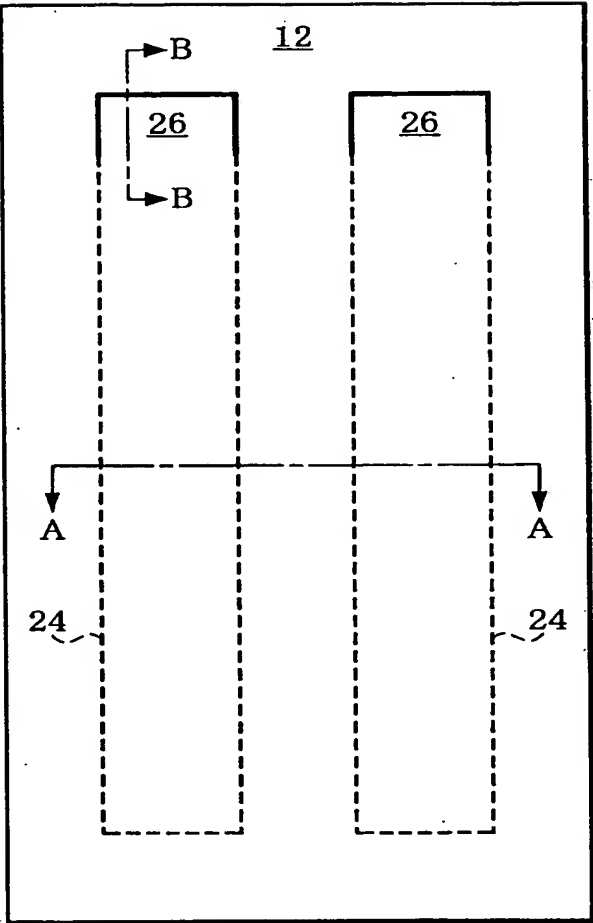


FIG.25

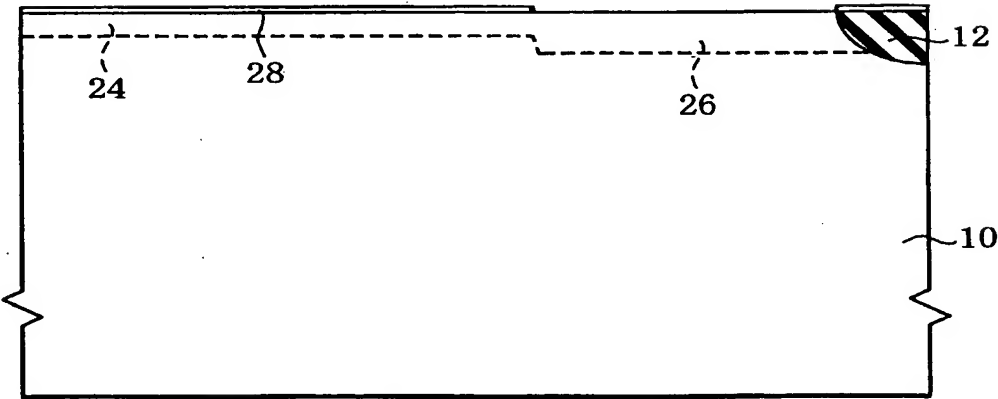


FIG.26

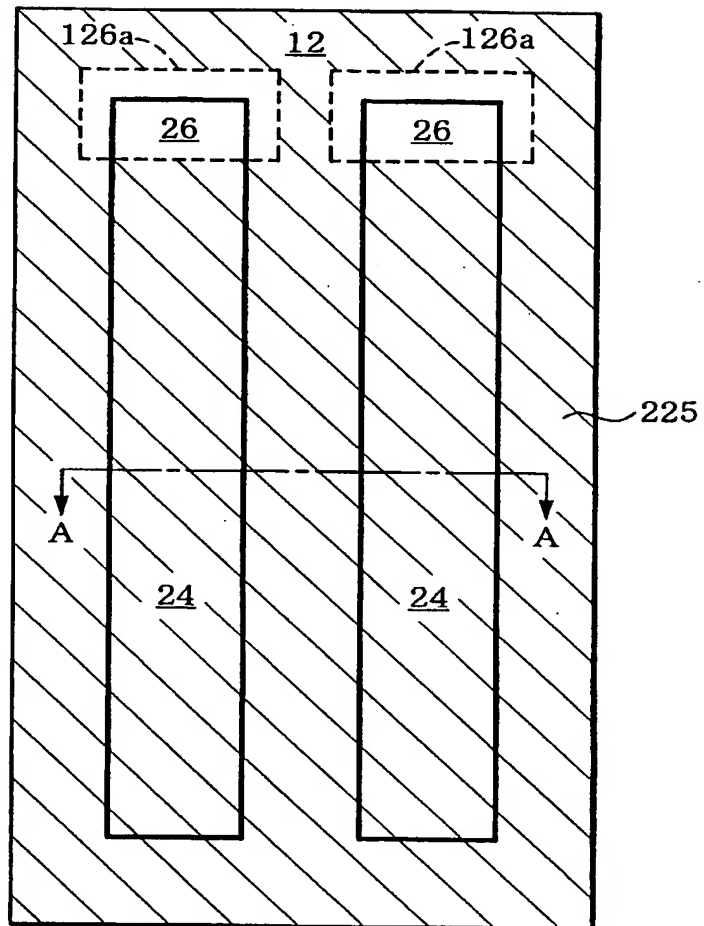


FIG.27

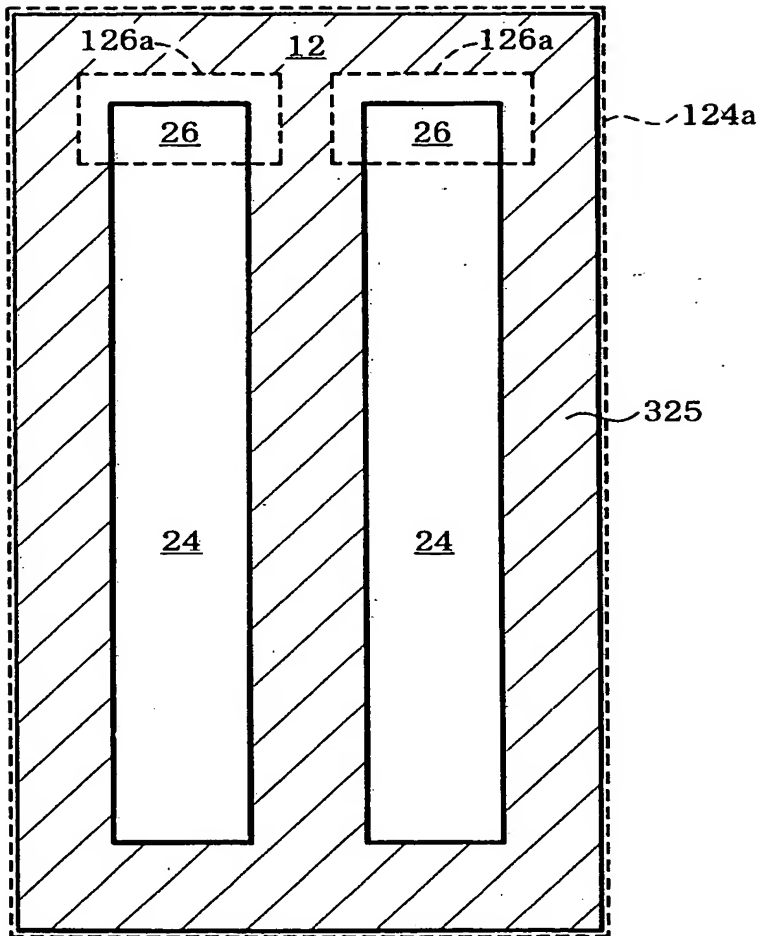


FIG.28

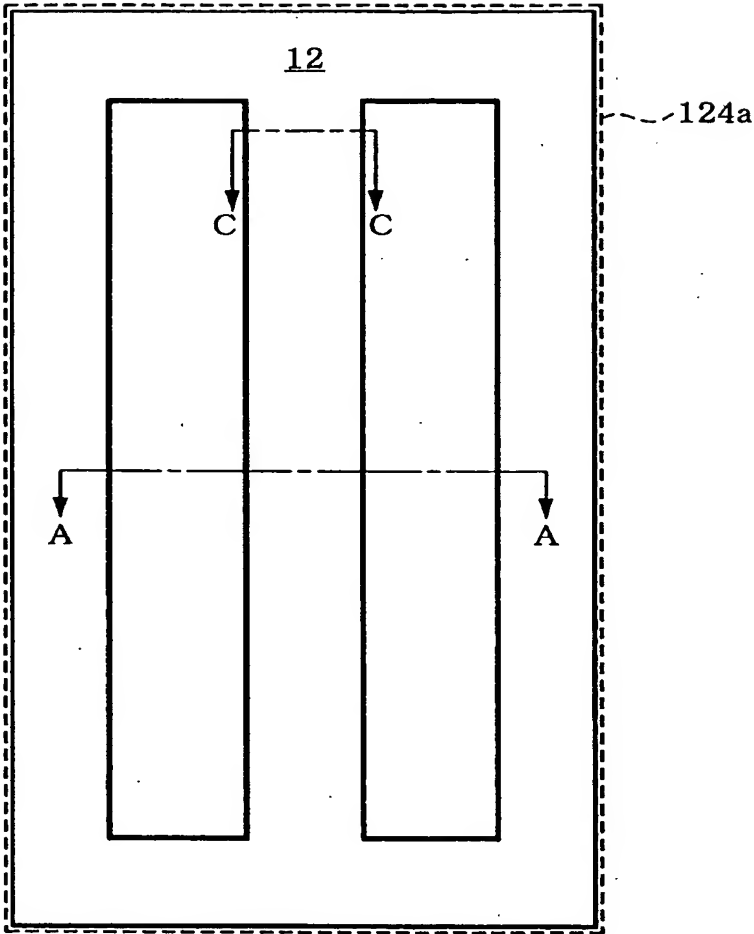


FIG.29

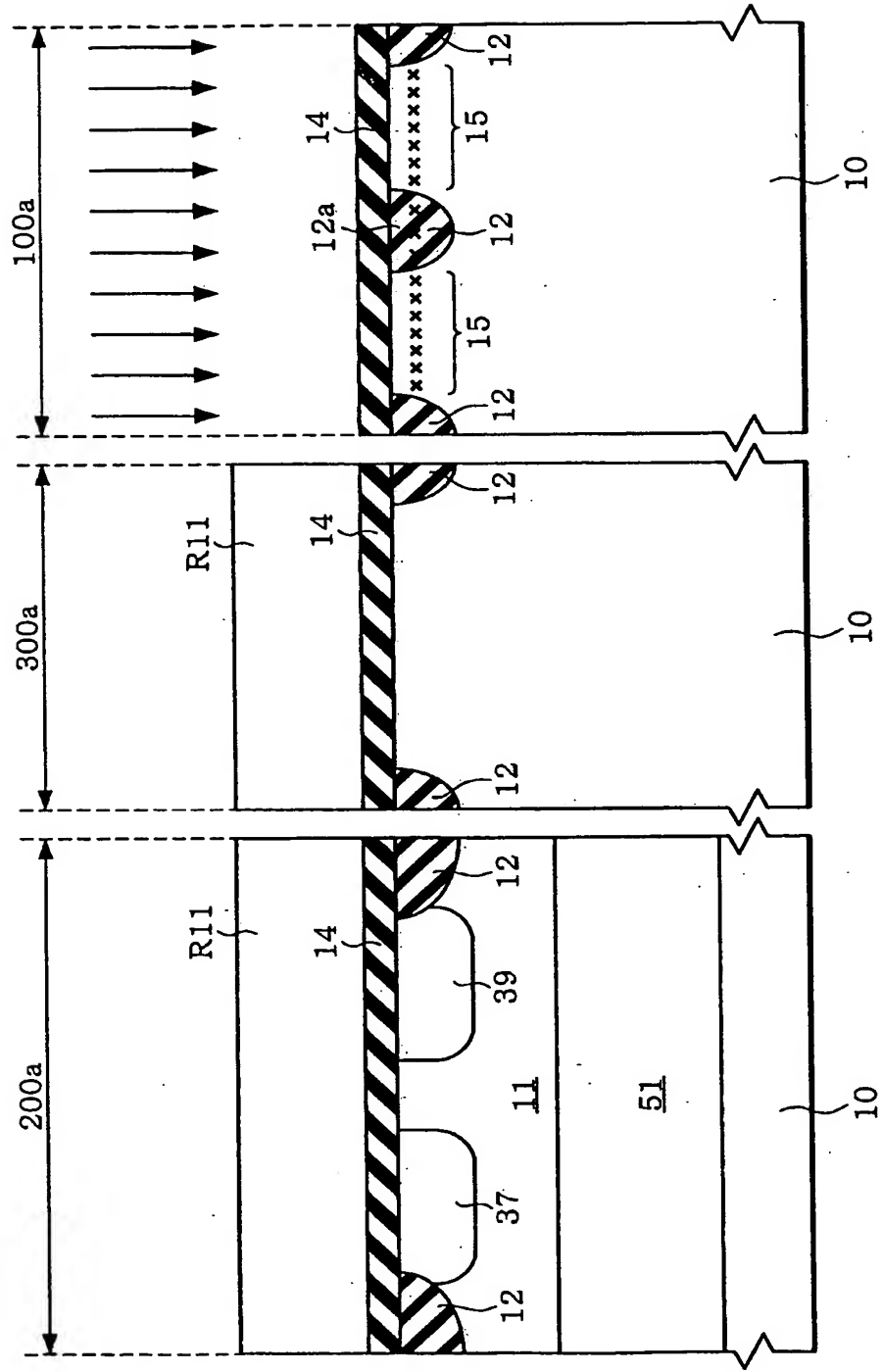


FIG.30

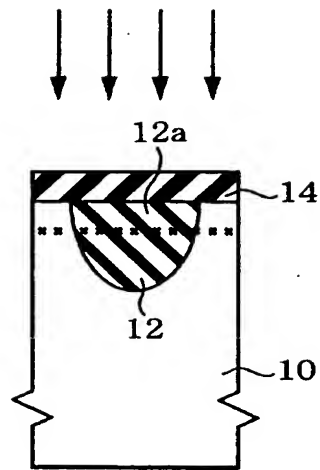


FIG.31

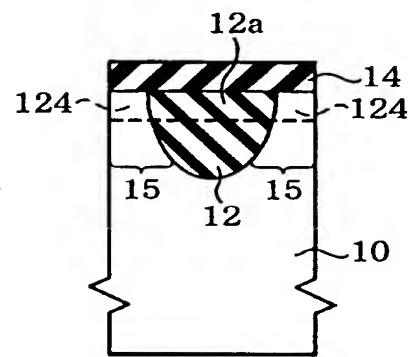


FIG.32

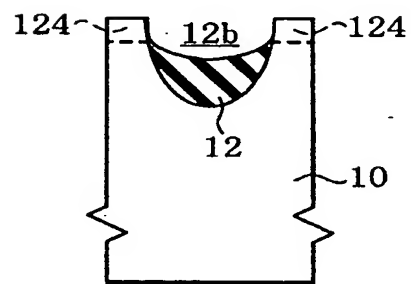


FIG.33

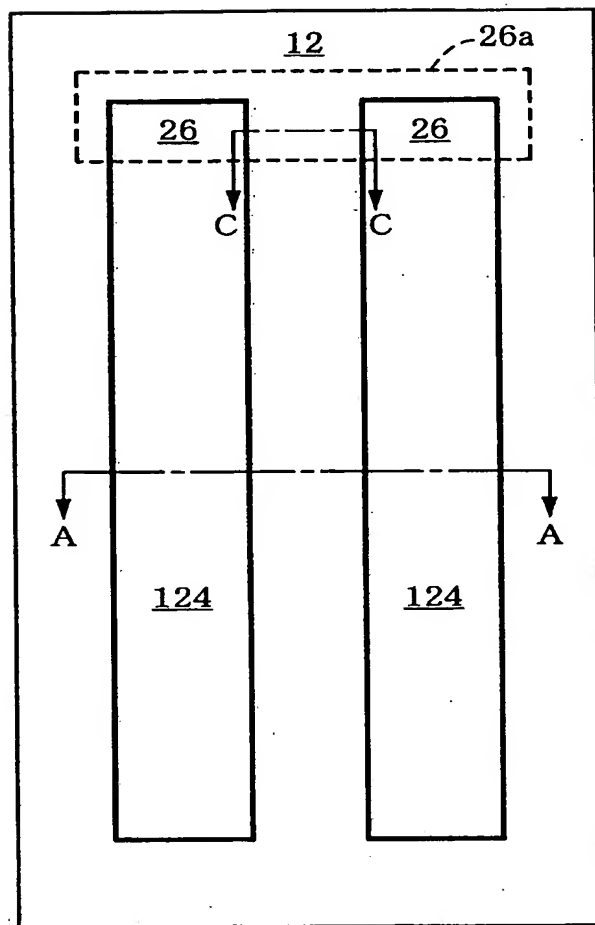


FIG.34

